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EXAMINER	
MUTSCHLER, BRIAN L	
ART UNIT	**PAPER NUMBER**
1753	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,176	SEO ET AL.	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 December 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 20011221.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: **28**, **32**, **35**, **36**, and **37** (see Figure 19). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

a. On page 6 at line 14, it appears that "non-electively" should be changed to --non-selectively--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7, 11, 14-16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Pan et al. (U.S. Pat. No. 5,011,580), with evidence of physical properties provided by "Polyimide," found at www.plasticsusa.com/tpi.html.

Regarding claim 1, Pan et al. disclose a method for forming interconnects in integrated circuits comprising the steps of:

a. depositing a metal seed layer **20** onto a partially fabricated integrated circuit device **10** (fig. 2; col. 3, lines 18-43);

b. depositing a photoresist **26** onto the metal seed layer **20** (fig. 3; col. 3, lines 44-46);

c. forming openings in the photoresist **26** by a photolithographic technique (fig. 4; col. 3, lines 47-57);

d. depositing metal **28** in the openings (fig. 5; col. 3, lines 58-63);

e. removing the photoresist layer **26** and the metal seed layer **20** (figs. 10 and 11; col. 3, line 64 to col. 4, line 19);

f. depositing a conformal barrier layer **34** onto the metal **28** (fig. 12; col. 4, line 53-56); and

g. depositing a dielectric material **40** onto the partially fabricated integrated circuit device **10** (fig. 13; col. 4, lines 57-68).

Regarding claim 2, the metal seed layer **20** is formed of a material to which the metal is directly plated (fig. 5; col. 3, lines 58-63).

Regarding claim 3, the metal seed layer **20** is copper (col. 3, lines 28-31).

Regarding claims 4 and 5, the metal **28** is formed by electroless plating or by electroplating (col. 3, lines 60-62).

Regarding claim 7, the barrier layer **34** can be selectively deposited by electroless plating (col. 4, lines 35-37).

Regarding claim 11, the barrier layer **34** is protective coating to protect the copper from oxidation and corrosion, and is thus an insulating layer (col. 4, lines 20-43).

Regarding claims 14-16, the dielectric material **40** is deposited by spin-coating (col. 4, lines 57-68). The dielectric material is polyimide, which is an organic polymer (col. 4, lines 57-68). As seen in "Polyimide," polyimide has a dielectric constant of 3.1, which is about 3.0.

Regarding claim 18, the method of Pan et al. further comprises the step of removing excess dielectric material **40** and the top portion of the barrier layer **34** to expose the top surface of the metal (fig. 14; col. 5, lines 1-13).

Regarding claim 19, the method of Pan et al. also repeats the steps (c)-(e) prior to depositing the barrier layer **34** (see figs. 7-10).

Regarding claim 20, the method further deposits a barrier layer **22** prior to step (a) (fig. 2; col. 3, lines 18-43).

Since Pan et al. teach all of the limitations recited in the instant claims, the reference is deemed to be anticipatory.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 7, 11, 14, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt et al. (U.S. Pat. No. 6,162,365) in view of Yew et al. (U.S. Pat. No. 6,159,845), with evidence of physical properties provided by "Copper Interconnect Films," found at www.appliedmaterials.com/products/copper_interconnect_films.html.

Regarding claim 1, Bhatt et al. disclose a method for forming interconnects in an integrated circuit comprising the steps of:

a. depositing a metal seed layer **14** on a partially fabricated integrated circuit device **12** (fig. 1; col. 2, line 66 to col. 3, line 13);

b. depositing a photoresist onto the metal seed layer **14** (col. 3, lines 36-53);

c. forming an opening in the photoresist by exposing to radiation (i.e., photolithography) (col. 3, lines 36-64);

d. depositing metal **40** in the openings (fig. 3; col. 3, line 65 to col. 4, line 6);

e. removing the photoresist and the metal seed layer **14** (fig. 5; col. 4, lines 22-48); and

f. depositing a conformal barrier layer **50** or **70** onto the metal layer **40** (fig. 6; col. 4, lines 54-60). Both layers **50**and **70** are capable of performing as barrier layers in the device. Although layer **50** is deposited before the

removal of the photoresist and the seed layer, the claimed method is open to such a method because the steps do not need to be performed in the recited order.

Regarding claim 2, the metal **40** is plated directly onto the seed layer **14** (col. 3, line 65 to col. 4, line 6).

Regarding claim 3, the metal seed layer **14** is copper (col. 3, lines 1-5).

Regarding claim 4, the metal **40** is deposited by electrolytic plating (col. 4, line 61 to col. 5, line 23).

Regarding claim 5, the metal **40** is deposited by an electroless plating process (col. 3, lines 65-66).

Regarding claim 7, the barrier layer **50** is deposited by electroless plating (col. 4, lines 7-9).

Regarding claim 11, the barrier layers **50** and **70** are insulators because they comprise noble or inert materials that insulate the metal **40** from corrosion.

The method of Bhatt et al. differs from the instant invention because Bhatt et al. do not disclose the following:

a. Depositing a dielectric material onto the partially fabricated integrated circuit device, as recited in claim 1.

b. The dielectric material is deposited by a chemical vapor deposition process, a physical vapor deposition process, or a spin-coating process, as recited in claim 14.

c. The dielectric material has a dielectric constant of less than about 3.0, as recited in claim 15.

d. The dielectric material comprises a carbon-doped silicate glass, and is deposited by a plasma-enhanced chemical vapor deposition process, as recited in claim 17.

Regarding claims 1, 14, 15, and 17, Yew et al. disclose a method disclose the formation of interconnects on an integrated circuit device, wherein the metal **130** is protected by a barrier cap **132** and a dielectric layer **134** (col. 3, line 53 to col. 4, line 4). The dielectric layer **134** is made of Black Diamond, manufactured by Applied Materials, which is deposited using plasma enhanced CVD (col. 3, line 66 to col. 4, line 4). Black Diamond is a carbon-doped silicate glass having a dielectric constant less than 3.0 (see "Copper Interconnect Films").

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Bhatt et al. to deposit a carbon-doped silicon film as a dielectric layer protecting the interconnect as taught by Yew et al. because the dielectric layer would protect the interconnects and electrically isolate the interconnects.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al. (U.S. Pat. No. 5,011,580), as applied above to claims 1-5, 7, 11, 14-16, and 18-20, and further in view of Hoinkis (U.S. Pat. No. 6,146,517).

Pan et al. disclose a method having the limitations recited in claims 1-5, 7, 11, 14-16, and 18-20 of the instant invention, as explained above in section 4.

Although Pan et al. teach that the copper metal can be electroplated, the method of Pan et al. differs from the instant invention because Pan et al. do not disclose the use of a plating bath comprising a dissolved cupric salt, as recited in claim 6.

Hoinkis teaches a method for forming copper interconnects in integrated circuits, wherein the method electroplates copper "in a standard fashion, for example using an electroplating bath comprising copper sulphate ($CuSO_4$) and sulphuric acid (H_2SO_4)" (col. 2, lines 18-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the copper electroplating method of Pan et al. to use a copper salt in the plating bath as taught by Hoinkis because a copper salt plating bath is the "standard fashion" for electroplating copper.

8. Claims 8-10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al. (U.S. Pat. No. 5,011,580) in view of Dubin et al. (U.S. 5,695,810).

Pan et al. disclose a method teaching the limitations recited in claims 1-5, 7, 11, 14-16, and 18-20 of the instant invention, as explained above in section 4.

Regarding claims 8, 10, and 13, Pan et al. teach that the barrier layer **34** may be chromium, nickel, a nickel alloy, or any other material that can be electrolessly

deposited (col. 4, lines 20-43). The purpose of the barrier layer **34** is to protect the copper **28** from oxidation and corrosion (col. 4, lines 20-43).

Regarding claim 13, Pan et al. further teach the formation of a barrier layer **41** and an interconnect bonding pad **42** on the interconnect (fig. 15; col. 5, lines 14-30). The bonding pad **42** insulates the barrier layer **41** from the exterior of the device (fig. 15).

The method of Pan et al. differs from the instant invention because Pan et al. do not teach the following:

a. The electroless plating process comprises the steps of depositing catalytic particles onto the surface of the metal and immersing the device into a plating bath, as recited in claim 8.

b. The catalytic particles are selected from a group consisting of palladium, cobalt, and nickel, and the plating bath comprises a hypophosphite reducing agent, as recited in claim 9.

c. The barrier layer is selected from a group consisting of CoWP, CoP, NiP, NiWP, CoB, NiB, and CoWB, as recited in claims 10 and 13.

d. The barrier layer is deposited by a chemical vapor deposition process or physical vapor deposition process, as recited in claim 12.

Regarding claims 8-10 and 13, Dubin et al. teach a method for forming copper interconnects on an integrated circuit, wherein a barrier layer is formed as a liner **15** and as an encapsulating layer **17** (fig. 5). Barrier layers made of CoWP are preferred because CoWP significantly enhances the barrier properties (col. 2, lines 53-65). Dubin

et al. further teach that catalytic material is deposited in a monolayer prior to the formation of the barrier layer material to activate the surface, and the catalytic material comprises palladium or cobalt (col. 5, lines 48-62). In addition, hypophosphite is used as a reducing agent (col. 48-62; col. 10, lines 5-9).

Regarding claim 12, Dubin et al. also teach that nickel and nickel alloys are known barrier layer materials and that PVD and CVD can be used to deposit barrier layer materials (col. 2, lines 45-57).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the electroless deposition of the barrier layer of Pan et al. to use an electroless plating process comprising the deposition of catalytic materials and a bath containing hypophosphite as taught by Dubin et al. because the catalytic materials and hypophosphite improve the electroless plating of the barrier layer. It also would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the barrier layer material of Pan et al. to use CoWP as taught by Dubin et al. because Dubin et al. teach that CoWP offers improved barrier characteristics over nickel barrier layers. Finally, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the deposition method of Pan et al. to use CVD or PVD when depositing the barrier layer because Dubin et al. teach that such techniques are known for the deposition of barrier layers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (571) 272-1341. The examiner can normally be reached on Monday-Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

blm
April 15, 2004

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